EK9713

Rev. 0.3

PRELIMINARY DATA SHEET

1200-Output TFT LCD Source Driver with TCON

fitipower integrated technology inc.

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1200-Output TFT LCD Source Driver with TCON

1. GENERAL DESCRIPTION

EK9713 is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. EK9713 is special designed for dual-gate architecture TFT panel. This chip is dedicated for the display resolution of: 800*480 and 800*600 application.

EK9713 input timing support TTL digital 24bit parallel RGB data format, and source output support 8-bit resolution 256 gray scales with dithering feature enabled. Operating parameters can be set via pin control for all control features. Special circuit architecture is designed for lower power dissipation.

EK9713 can be configured as dual-gate operation mode for reducing FPC amount and save the cost. With wide range of supply voltages and many pin control features make this chip more suitable for various applications.

2. FEATURES

- Special design for small-sized color TFT LCD source drivers with timing controller
- Integrated 1200 channel source driver
- Support dual-gate operation mode
- Support display resolutions : 800(RGB)x480、800(RGB)x600
- Support TTL 24-bit parallel (RGB) input timing
- Source output with 8-bit resolution 256 gray scale (2-bit dithering)
- Support Delta or Stripe color filter configuration
- Support stand-by mode for low power consumption
- Pin controlled UP/DOWN, LEFT/RIGHT, HV/DE mode select function
- Embedded Gamma Table for special custom request
- Support external V1 ~ V14 pad for Gamma adjusting
- Output dynamic range: 0.1 ~ AVDD-0.1V
- Power for source driver voltage AVDD: 6.5V ~ 13.5V
- Power for digital interface circuit VDD: 3.0 ~ 3.6V
- Max. operating frequency: 50 MHz
- COG package

3. BLOCK DIAGRAM

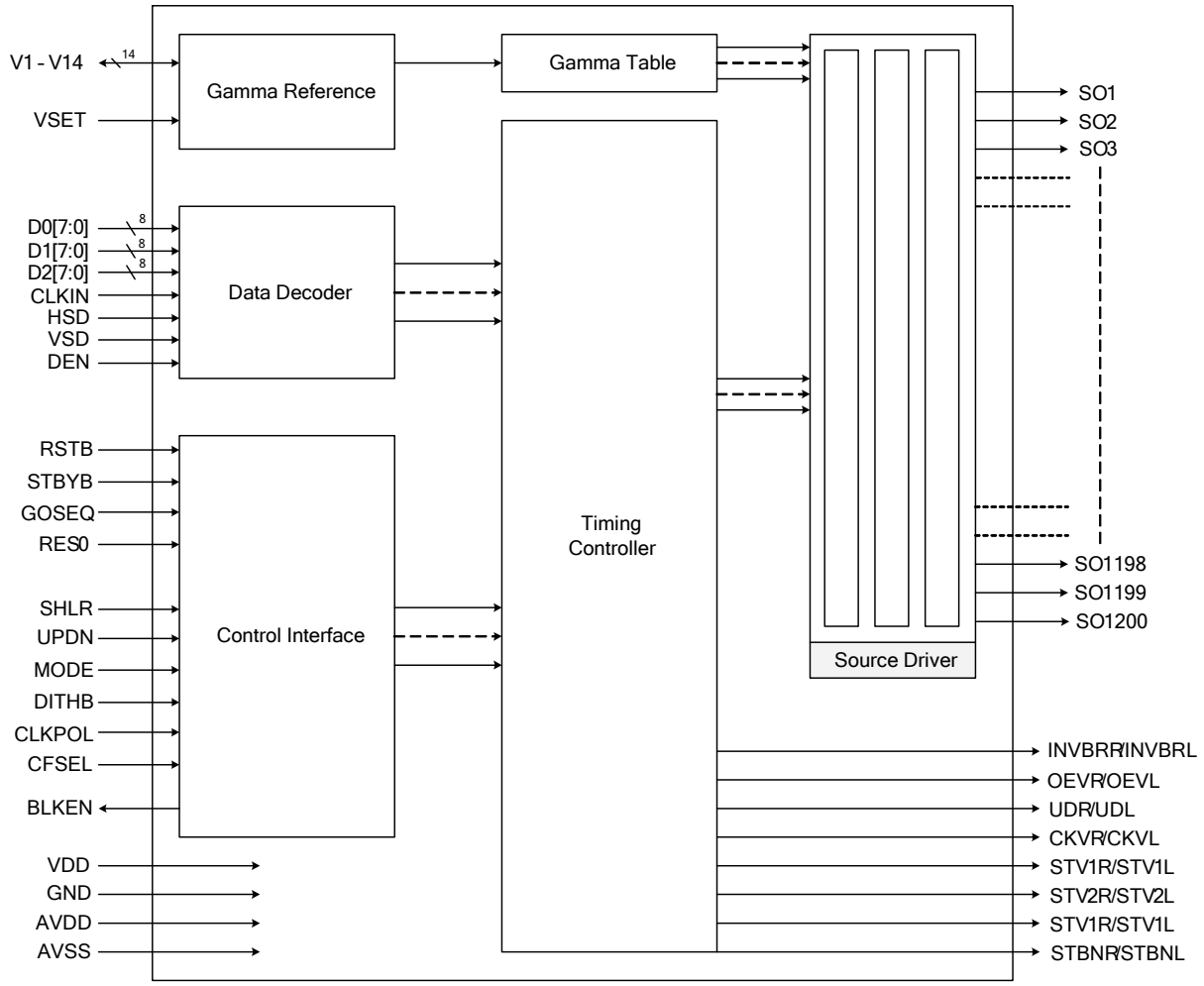


Figure 1. Block Diagram

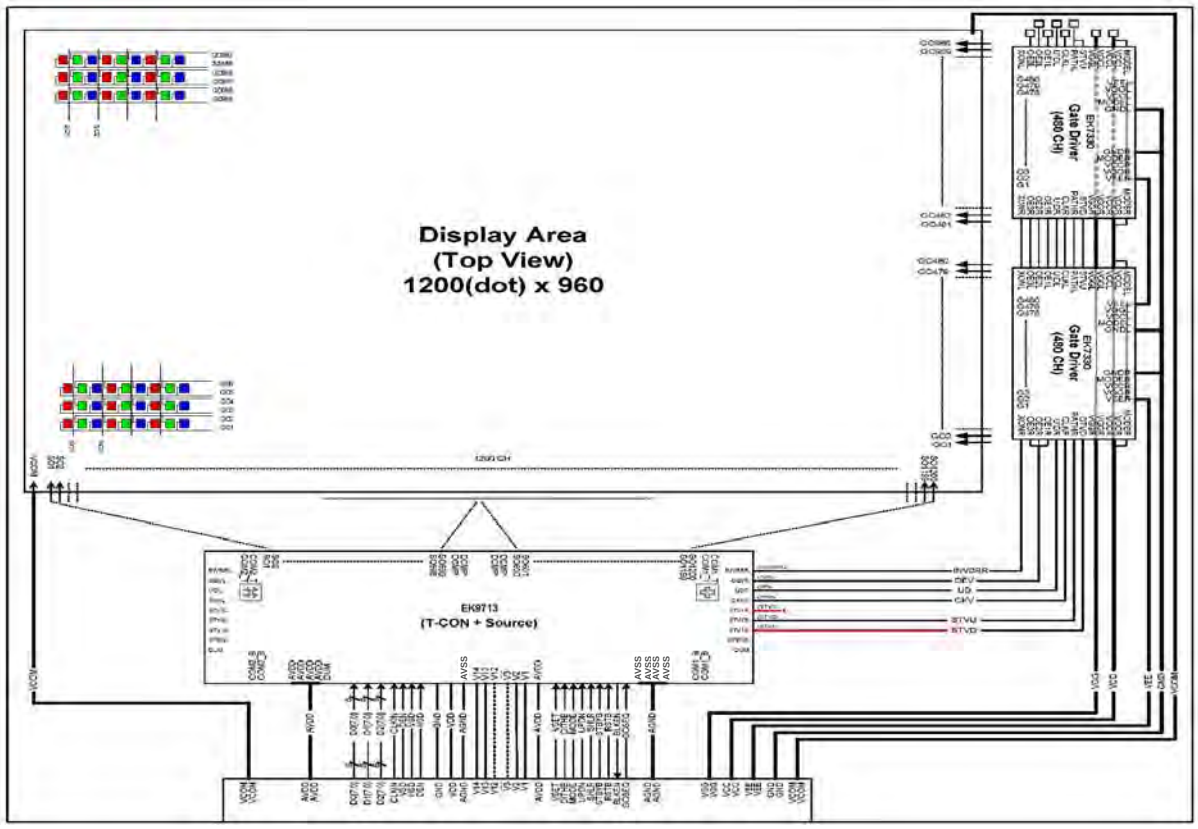


Figure 2. Application Block Diagram – Dual Gate Application

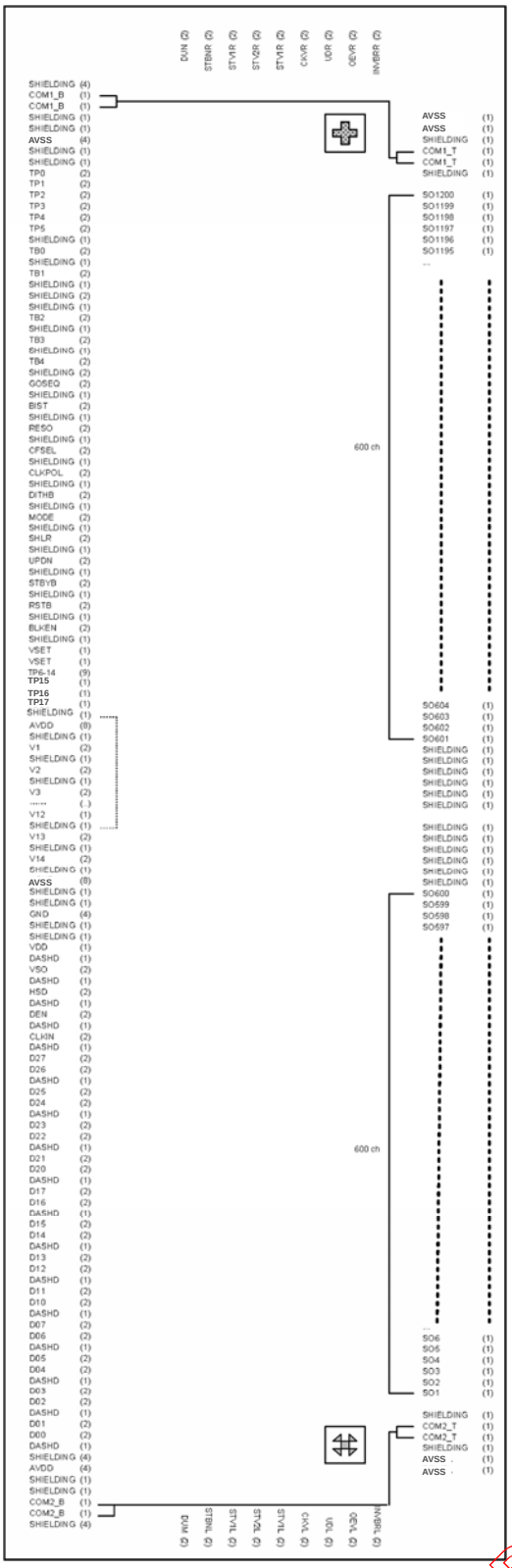


Figure 3. Pad Sequence (Bump Side)

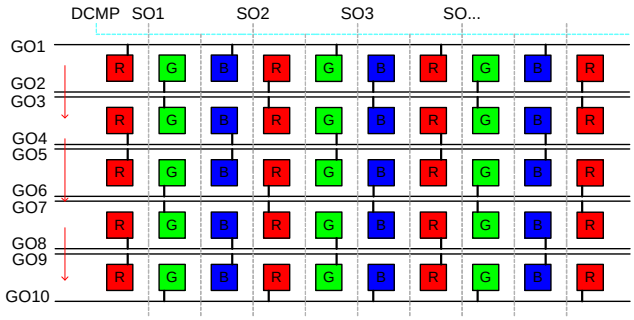
4. PIN DESCRIPTION

Table 1. Pin Description

Pin Name	Pin Type	Description
D07~D00 D17~D10 D27~D20	Input	Parallel data Input. For TTL 24-bit parallel RGB image data input. D[07:00] = R[7:0] data; D[17:10] = G[7:0] data; DIN[27:20] = B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to GND.
CLKIN	Input	Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge.
HSD	Input	Horizontal Sync input. Negative polarity. Normally pull high.
VSD	Input	Vertical Sync input. Negative polarity. Normally pull high.
DEN	Input	Data Input Enable. Active High to enable the data input bus under “DE Mode”. Normally pull low.
MODE	Input	DE / SYNC mode select. Normally pull high H: DE mode. L: HSD/VSD mode.
RES0	Input	Display resolution selection. RES0 = “0”, for 800(RGB)*480 display resolution RES0 = “1”, for 800(RGB)*600 display resolution
DITHB	Input	Dithering function enable control. Normally pull high DITHB = “1”, Disable internal dithering function DITHB = “0”, Enable internal dithering function
CLKPOL	Input	Input clock edge selection. Normally pull low CLKPOL = “1”, Latch data at CLKIN rising edge. CLKPOL = “0”, Latch data at CLKIN falling edge. (Default)
BLKEN	Output	Backlight enable control signal for external controller. BLKEN = “1”, Logical control signal to turn on external backlight controller BLKEN = “0”, Turn off external backlight controller Note: Refer to the Power On/Off Sequence for the detail information.
CFSEL	Input	Color Filter type selection. Normally pull high CFSEL = “1”, Stripe mode. (Default) CFSEL = “0”, Delta mode
V1 ~ V14	Bi-direction	When VSET=”0”, INTERNAL Gamma Table is used. V1~V14 pad are un-used. When VSET=”1”. V1~V14 are the external gamma correction points. The voltage of these pins must be: AVSS<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1<AVDD
VSET	Input	Gamma correction source select. Normally pull low. VSET = ”0”, use internal Gamma Reference voltage (AVDD). (Default mode) VSET = ”1”, use external Gamma Correction Input (V1~V14).
RSTB	Input	Global reset pin. Active Low to enter Reset State. Suggest to connecting with an RC reset circuit for stability. Normally pull high.
STBYB	Input	Standby mode, Normally pull high. STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z

Pin Name	Pin Type	Description
SHLR	Input	Source Right or Left sequence control. Normally pull high. SHLR = “L”, shift left: last data = S1←S2←S3.....←S1200 = first data. SHLR = “H”, shift right: first data = S1→S→S3.....→S1200 = last data.
UPDN	Input	Gate Up or Down scan control. Normally pull low. UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver. UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.
BIST	Input	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
GOSEQ	Input	Gate on sequence. Normally pull low. Please refer to Note. GOSEQ = H : INVBRR/INVBRL = L Gate on G1→G2→G4→G3→G5→G6→G8→G7……. GOSEQ = L : INVBRR/INVBRL = H Gate on G1→G2→G3→G4→G5→G6→G7→G8…….
OEVR/OEVL	Output	Gate driver control signal.
UDR/UDL	Output	Gate driver control signal.
CKVR/CKVL	Output	Gate driver control signal.
STV1R/STV1L	Output	Gate driver control signal.
STV2R/STV2L	Output	Gate driver control signal.
STBNR/STBNL	Output	Gate driver control signal.
INVBRR/INVBRL	Output	Gate driver control signal (For special Gate on sequence).
AVDD	Power Input	Power supply for analog circuits
AVSS	Power Input	Ground pins for analog circuits
VDD/VDDD	Power Input	Power supply for digital circuits
GND/VSSD	Power Input	Ground pins for digital circuits
SO1~SO1200	Output	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
ALIGN	Mark	For assembly alignment.
COM1_B COM1_B	Shorted line	Internal link together between input side and output side.
COM1_T COM2_T	Shorted line	Internal link together between input side and output side.
TP17~0 TB0~4	Testing	Float these pins for normal operation.
SHIELDING	Shielding	IC Shielding pads. Those pins are internally connected to the AVSS. DO NOT connect to any WOA on the panel.
DASHD	Shielding	Data Bus Shielding pad. Those pins are internally connected to the GND. RECOMMAND to add shielding lines on the FPC to reduce EMI.
DUM	Dummy	Dummy pads. Those pins are floating pads.

GOSEQ = L, INVBRRINVBRL= H,
With traditional Gate driver.



GOSEQ = H, INVBRRINVBRL= L,
With special design Gate driver

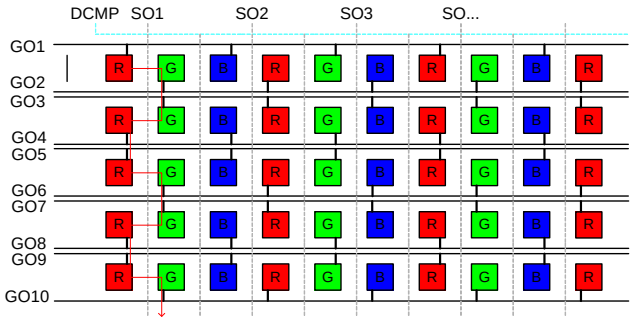


Table 2. EK9713 Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_B	COM1_T
2	COM2_B	COM2_T

4.1. Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Table 3.

Pin Name	Wiring Resistance value(Ω)	Pin Name	Wiring resistance value (Ω)
AVDD	<5	SHLR	<500
AVSS	<5	UPDN	<500
VDD	<10	BIST	<500
GND	<10	MODE	<500
V1~V14	<10	RES0	<500
D00~D07	<50	CLKPOL	<500
D10~D17	<50	BLKEN	<500
D20~D27	<50	CFSEL	<500
CLKIN	<50	VSET	<500
VSD	<50	OEVx	<500
HSD	<50	UDx	<500
DEN	<50	CKVx	<500
RSTB	<500	STV1x	<500
STBYB	<500	STV2x	<500
DITHB	<500	STBNx	<500

5. FUNCTION DESCRIPTION

5.1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

This is another paragraph of sub-function description.

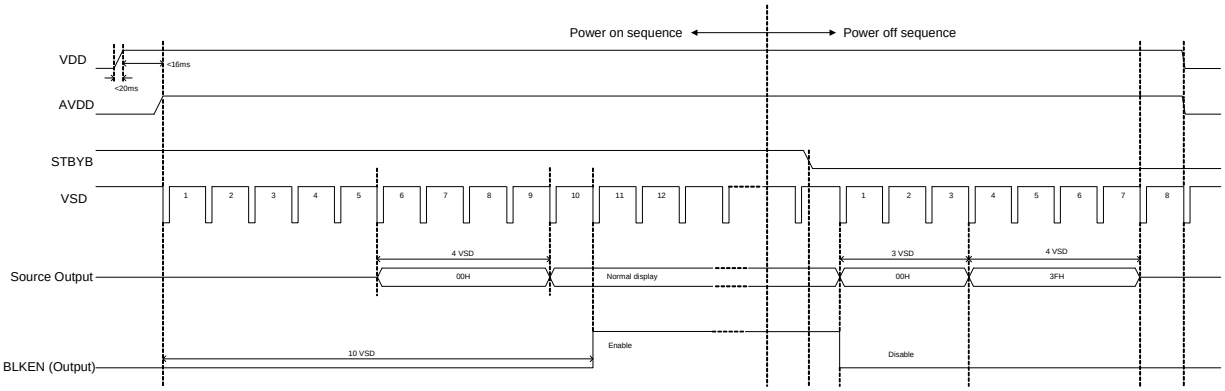


Figure 4. Power-On/Off Timing Sequence

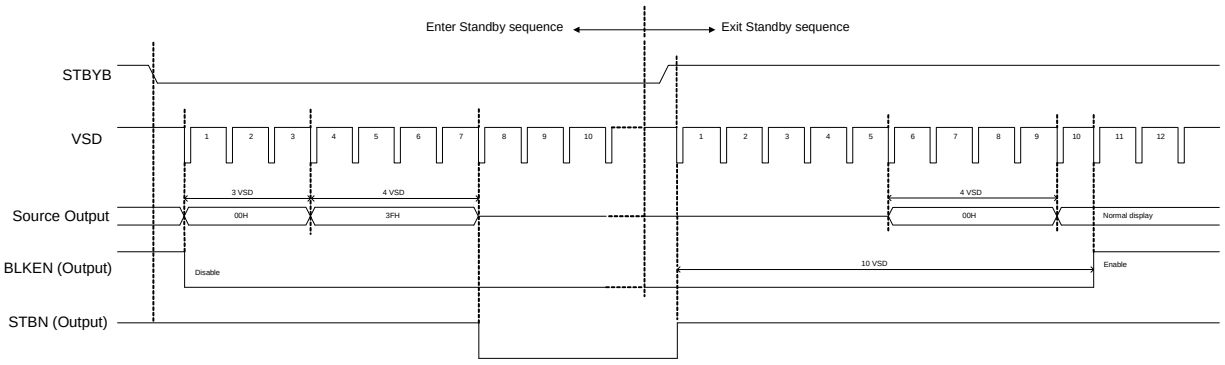


Figure 5. Enter and Exit Standby Mode Sequence

5.2. Input Data VS Output Channels

5.2.1. CFSEL="1", Stripe Mode, UDPN=1

Table 4. SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line/Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line/Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Even Line/Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

Table 5. SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line/Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line/Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Even Line/Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20

5.2.2. CFSEL="0", Delta Mode, UDPN=1

Table 6. SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line/Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line/Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/Gn	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/Gn+1	D27~D20	D17~D10	D07~D00	---	D27~D20	D17~D10	D07~D00

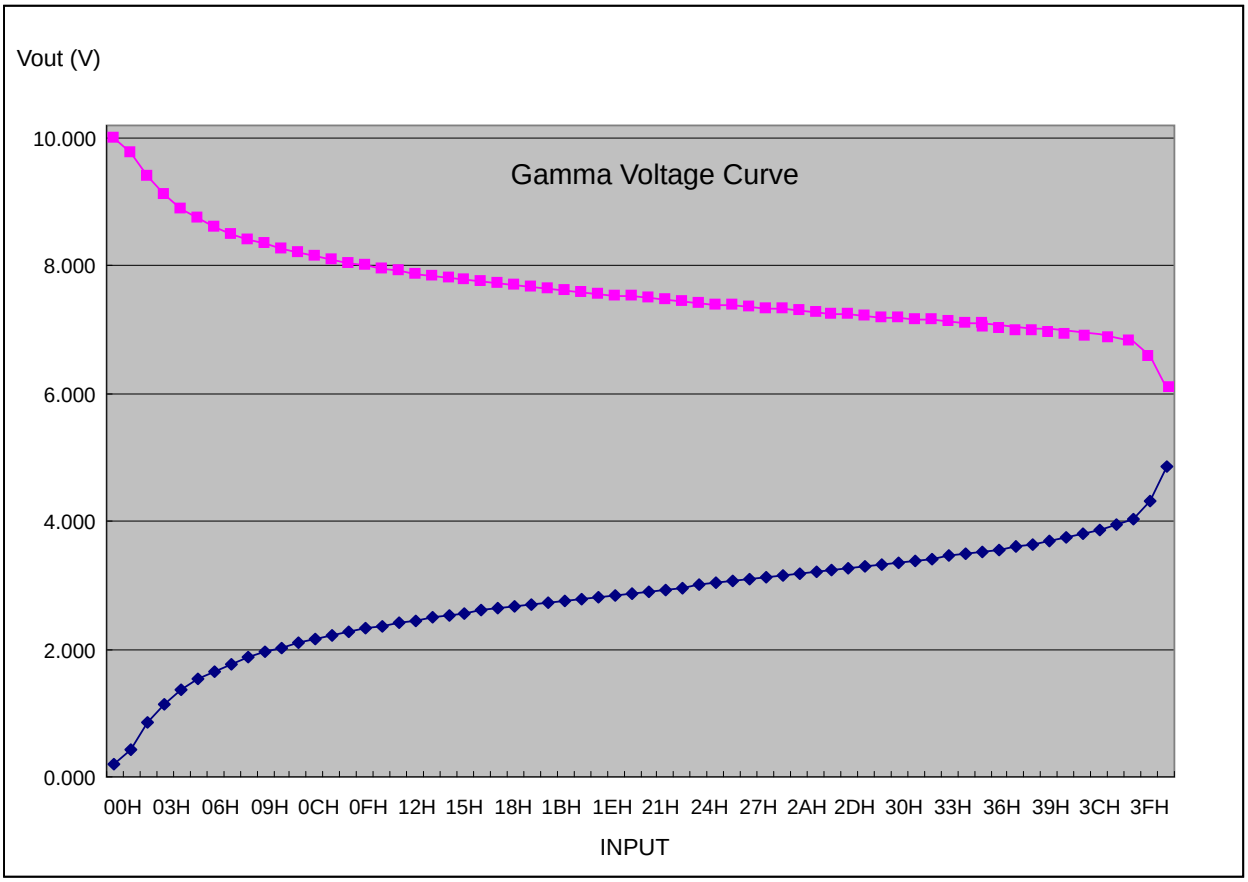
Table 7. SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line/Gn	D07~D00	D27~D20	D17~D10	---	D07~D00	D27~D20	D17~D10
Odd Line/Gn+1	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/Gn	D17~D10	D07~D00	D27~D20	---	D17~D10	D07~D00	D27~D20
Even Line/Gn+1	D27~D20	D17~D10	D07~D00	---	D27~D20	D17~D10	D07~D00

5.3. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

Gamma Tables very for each customer.



Remark: AVDD-0.1 > V1 > V2> V3 > V4 > V5 > V6 > V7; V8 > V9 > V10 > V11 > V12 > V13 > V14 > AVSS+0.1V

5.4. Input Data and Output Voltage Reference Table

Table 8. Input Data and Output Voltage Reference Table

Asy-Gamma @AVDD=10.4V					
Level	**V+**	**V-**	**Level**	**V+**	**V-**
0	9.99544	0.19544	32	7.62801	2.96276
1	9.74167	0.46609	33	7.6064	2.99432
2	9.38791	0.84598	34	7.58521	3.02776
3	9.14826	1.10631	35	7.56694	3.05722
4	8.959	1.31459	36	7.54802	3.0877
5	8.81096	1.47967	37	7.52618	3.11692
6	8.69215	1.61326	38	7.50274	3.14577
7	8.59155	1.7279	39	7.48152	3.17187
8	8.50539	1.82725	40	7.46153	3.20067
9	8.42879	1.91694	41	7.44259	3.23201
10	8.3584	1.99876	42	7.43079	3.27186
11	8.30101	2.06792	43	7.41956	3.30901
12	8.24502	2.13436	44	7.40122	3.34041
13	8.19379	2.19625	45	7.38502	3.37533
14	8.14825	2.252	46	7.36578	3.4085
15	8.10377	2.30712	47	7.34928	3.44419
16	8.0645	2.35712	48	7.32513	3.4736
17	8.02666	2.40518	49	7.30037	3.50375
18	7.98939	2.45231	50	7.28065	3.54065
19	7.95731	2.49381	51	7.26167	3.58033
20	7.92413	2.53902	52	7.24646	3.62519
21	7.89613	2.58001	53	7.22793	3.66813
22	7.86902	2.61944	54	7.21236	3.72165
23	7.8407	2.66138	55	7.19252	3.77243
24	7.81479	2.69689	56	7.17277	3.82699
25	7.78911	2.73111	57	7.15248	3.89333
26	7.76239	2.76723	58	7.1318	3.96111
27	7.73804	2.80206	59	7.10615	4.04641
28	7.716	2.83394	60	7.07255	4.13526
29	7.69307	2.8673	61	7.01529	4.24283
30	7.6691	2.90199	62	6.9063	4.39937
31	7.64845	2.93198	63	6.28445	5.08445

Note: Gamma Tables Vary for each customer.

5.5. Data Input Format

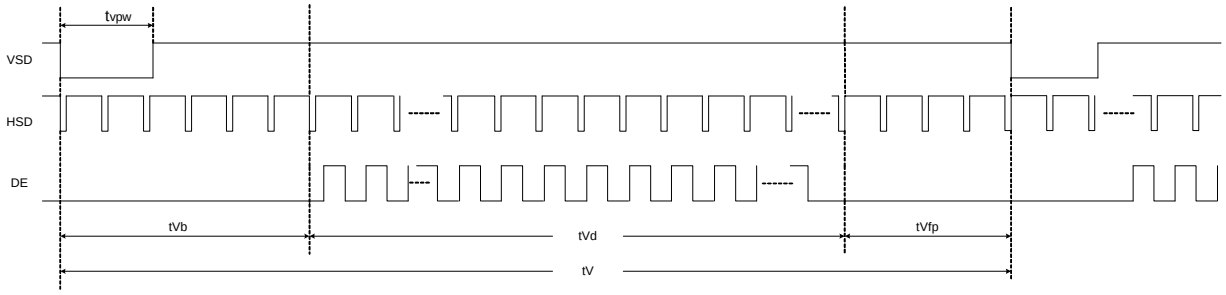


Figure 6. Vertical input timing

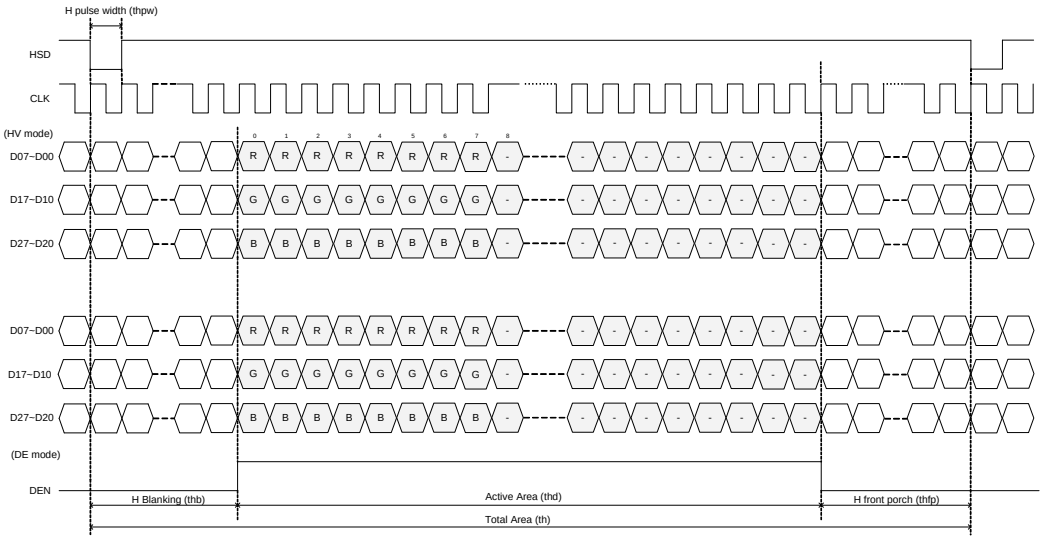


Figure 7. Horizontal input timing

5.6. Timing Characteristic

5.6.1. For 800 × 480 panel

Table 9. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency		fclk	Min.	Typ.	Max	
			-	33.3	50	MHz
1 Horizontal Line		th	862	1056	1200	DCLK
HSD pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			40		
HSD Back Porch (Blanking)		thb	46	46	46	
HSD Front Porch		thfp	16	210	354	

Table 10. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical display area	tvd		480		H
VSD period time	tv	510	525	650	H
VSD pulse width	tvpw	1	-	20	H
VSD Back Porch (Blanking)	tvb	23	23	23	H
VSD Front Porch	tvfp	7	22	147	H

5.6.2. For 800 × 600 panel

Table 11. Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		800		DCLK
DCLK frequency		fclk	Min.	Typ.	Max	
			-	40	50	MHz
1 Horizontal Line		th	862	1056	1200	DCLK
HSD pulse width	Min.	thpw		1		
	Typ.			-		
	Max.			40		
HSD Back Porch (Blanking)		thb	46	46	46	
HSD Front Porch		thfp	16	210	354	

Table 12. Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical display area	tvd		600		H
VSD period time	tv	624	635	700	H
VSD pulse width	tvpw	1	-	20	H
VSD Back Porch (Blanking)	tvb	23	23	23	H
VSD Front Porch	tvfp	1	12	77	H

6. ELECTRICAL SPECIFICATION

6.1. Absolute Maximum Ratings

Table 13. VOLTAGE (TA = 25°C, GND = AVSS = 0V)

	Min.	Max.	Unit
Digital Supply Voltage, VDD	-0.5	+5.0	V
Analog Supply Voltage, AVDD, V1~V14	-0.5	+15.0	V

Table 14. TEMPERATURE

	Min.	Max.	Unit
Operating temperature	-20	+85	°C
Storage temperature	-55	+125	°C

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. Recommended Operating Range

Table 15. Recommended Operating Range (TA = -20 to 85°C, GND = AVSS = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	3.0	3.3	3.6	V
Analog supply voltage	AVDD	6.5	-	13.5	V
Digital input voltage	VIN	0	-	VDD	V

6.3. DC Characteristics

Table 16. DC Characteristics

(TA = -20 to 85°C, VDD = 3.0 to 3.6V, AVDD = 6.5 to 13.5V, GND = AVSS = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD-0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	GND+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD=3.3V	150K	250K	350K	ohm
Digital Operation current	Idd	Fclk=40 MHz, FLD=37.88KHz, VDD=3.3V	-	8	10	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=40MHz, FLD=37.88KHz @ AVDD=10V,V1=8V, V14=0.4V	-	10	12	mA
Analog Stand-by current	Ist2	No load, Clock and all functions are stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input	0.4*AVDD	-	AVDD-0.1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input	0.1	-	0.6*AVDD	V
Output Voltage deviation	Vod1	Vo = AVSS+0.1V ~ AVSS+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AVSS+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AVSS+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ SO1200	0.1	-	AVDD-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ SO1200; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ SO1200; Vo=13.4V v.s 12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

6.4. AC Characteristics

Table 17. AC Characteristics

(TA = -20 to 85°C, VDD = 3.0 to 3.6V, AVDD = 6.5 to 13.5V, GND = AVSS = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD Power On Slew rate	TPOR	From 0V to 90% VDD	-	-	20	ms
RSTB pulse width	TRST	CLKIN = 40MHz	1	-	-	ms
CLKIN cycle time	Tcph	-	20	-	-	ns
CLKIN pulse duty	Tcwh	-	40	50	60	%
VSD setup time	Tvst	-	8	-	-	ns
VSD hold time	Tvhd	-	8	-	-	ns
HSD setup time	Thst	-	8	-	-	ns
HSD hold time	Thhd	-	8	-	-	ns
Data set-up time	Tdsu	D0[7:0], D1[7:0], D2[7:0] to CLKIN	8	-	-	ns
Data hold time	Tdhd	D0[7:0], D1[7:0], D2[7:0] to CLKIN	8	-	-	ns
DEN setup time	Tesu	-	8	-	-	ns
DEN hold time	Tehd	-	8	-	-	ns
Output stable time	Tsst	10% to 90% target voltage. CL=120pF, R=10K ohm	-	-	6	us

6.5. Timing Table

Table 18. Parallel 24-bit RGB Mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKIN Frequency	Fclk	VDD = 3.0V ~3.6V	-	33.3	50	MHz
CLKIN Cycle Time	Tclk	-	20	30	-	ns
CLKIN Pulse Duty	Tcwh	Tclk= Tcwh + cwl	40	50	60	%
	Tcwl		40	50	-60	%
VSD to STV	Tstv	HV mode	-	24	-	H
DEN to STV	Tstv	DE mode	-	4	-	CLKIN
STV pulse width	Twstv	-	-	0.5	-	H
STV to CKV	Tckv	-	-	18	-	CLKIN
STV to OEV	Toev	-	-	2	-	CLKIN
CKV Pulse Width	Twckv	-	-	66	-	CLKIN
OEV Pulse Width	Twoev	-	-	50	-	CLKIN

6.6. Timing Waveform

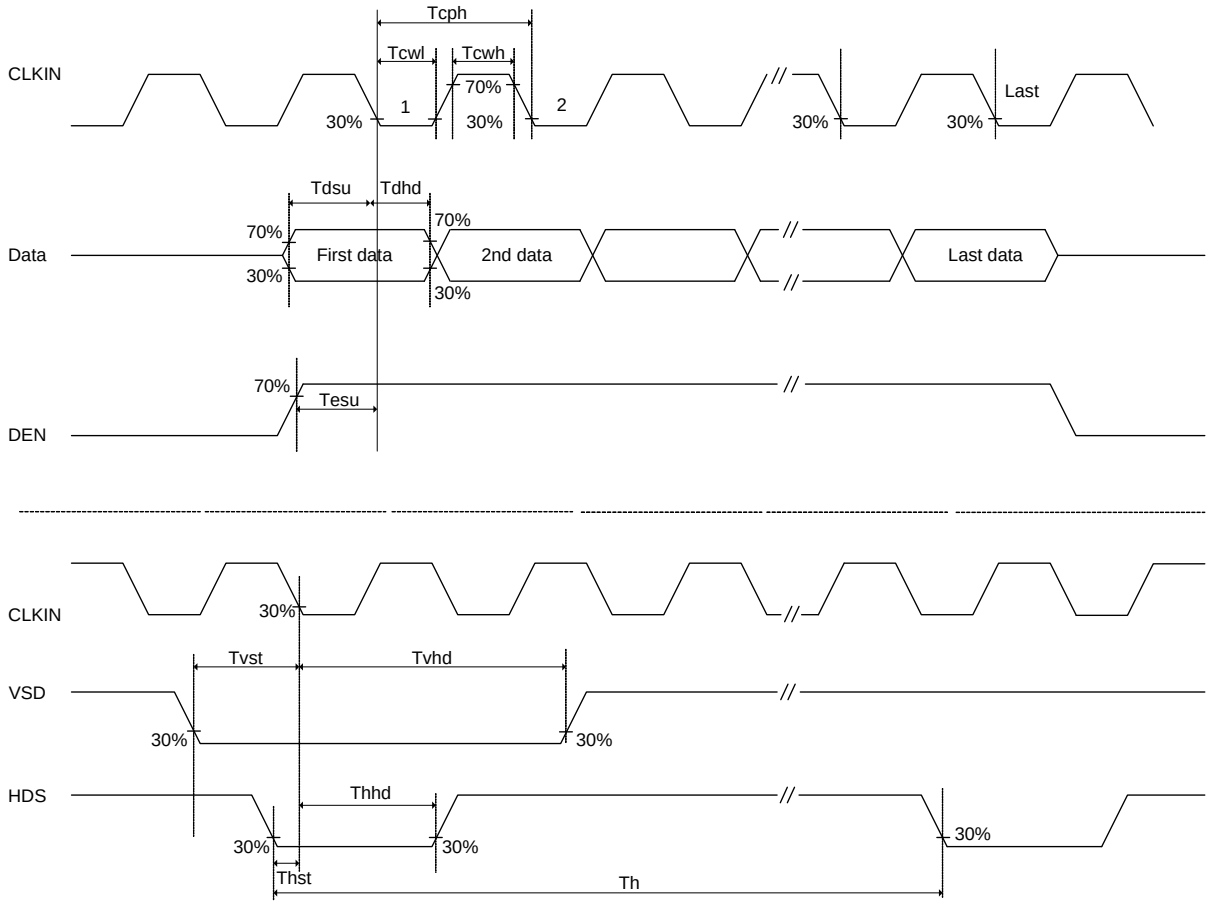


Figure 8. Input Clock and Data Timing Diagram

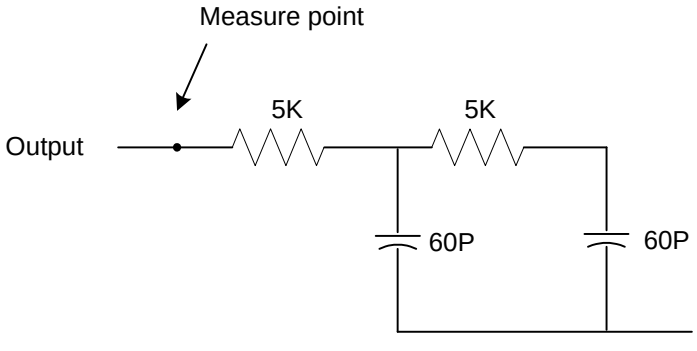


Figure 9. Output load condition

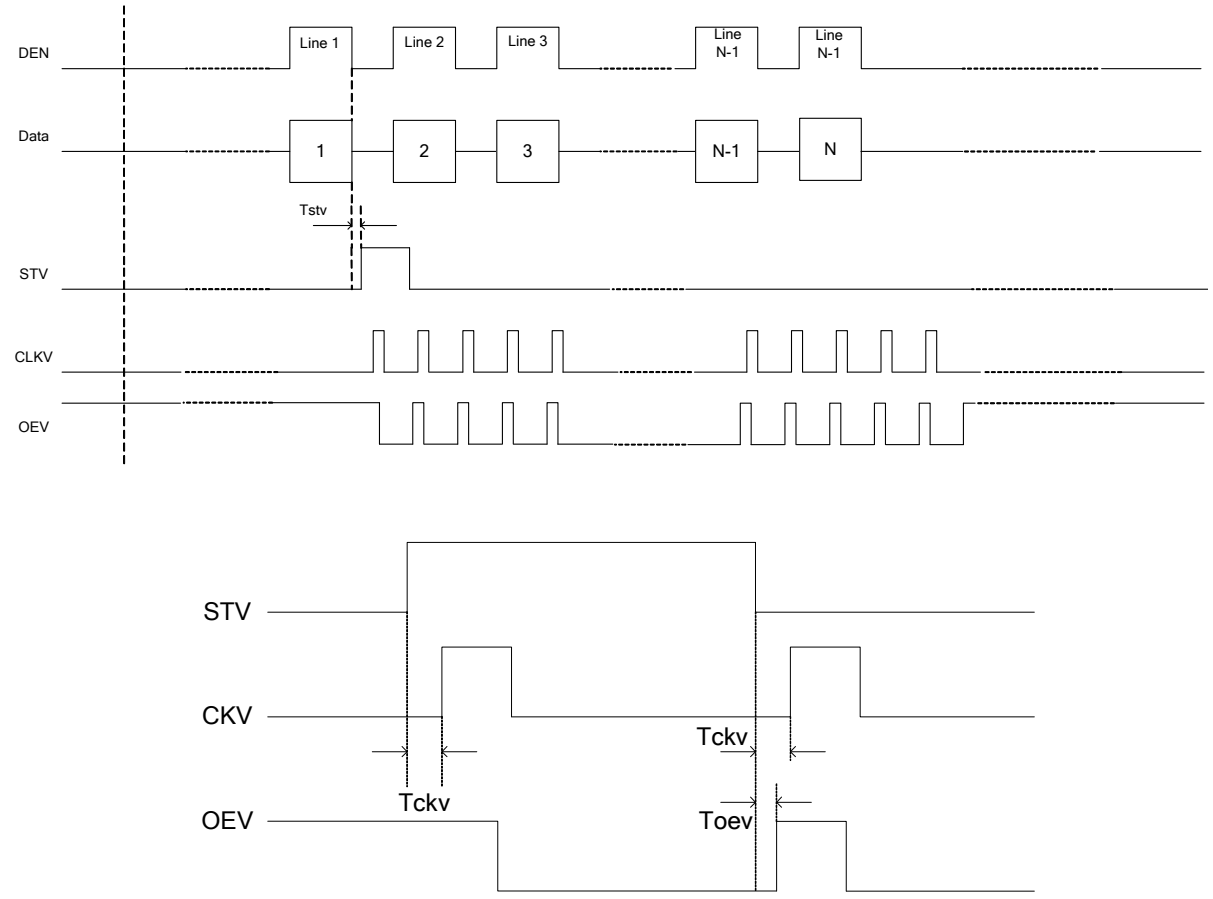


Figure 10. Vertical Timing Diagram DE

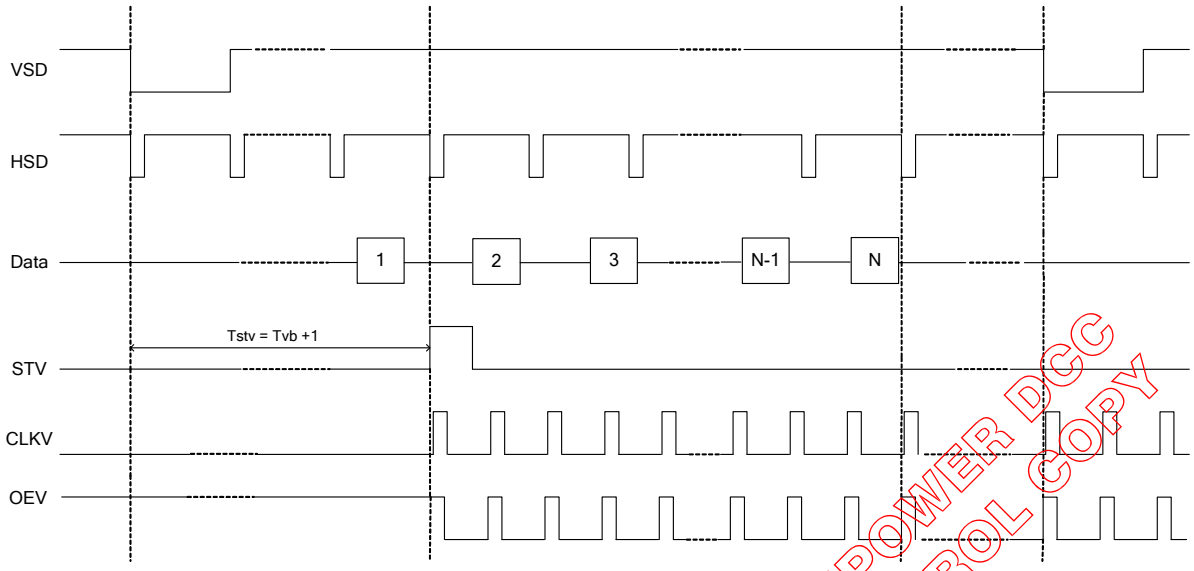


Figure 11. Vertical Timing Diagram HV

7. DEFINITIONS

7.1. Data Sheet Status

Preliminary Data Sheet	This data sheet contains preliminary data; supplementary data may be published later.
Data Sheet	This data sheet contains final product specifications.

Contents in the document are subject to change without notice.

7.2. Life Support Application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. fitipower customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify fitipower for any damages resulting from such improper use or sale.

8. REVISION HISTORY

Revision	Content	Date
0.1	New Issue.	2008/8/19
0.2	1. Update Gamma Table. 2. Fix DCMPR, DCMPL pads to AVSS.	2008/12/9
0.3	1. 5.2.1 CFSEL="1", Stripe Mode,→ CFSEL="1", Stripe Mode, UDPN=1 2. 5.2.2 CFSEL="0", Delta Mode, → CFSEL="0", Delta Mode, UDPN=1	2009/4/9